REMARKS

As an initial matter, Applicants appreciate the Examiner's acknowledgement that claims 2-7, 9-14, and 16-21 contain allowable subject matter. For the reasons that follow, reconsideration and withdrawal of all outstanding rejections and objections are requested.

Claims 22-23 have been withdrawn. The Office Action maintains the previous restriction requirement of these claims, stating that searching the method "of forming a semiconductor device requires a different thought process and class in searching than the semiconductor device structure." Office Action, at 2. Claim 23, however, relates to a semiconductor device, not a method of formation. For at least this reason, Applicants respectfully request that the Examiner reconsider this restriction, at least with respect to claim 23.

Claims 1, 6, 13-15, and 20-21 stand objected to because of what the Office Action states is an informality with respect to the described location of the drain for the P-channel DMOS transistor. Specifically, the Examiner states that the word "of" should be replaced with "in." Applicants respectfully disagree. Applicants would direct the Examiner's attention to the Specification, at p. 27, lines 17-21, with reference to an exemplary embodiment of the invention, as shown in FIG. 3. There, it is explained that the "p-type low concentration epitaxial layer 4 and the P-type high concentration semiconductor substrate 2 serve as drains of the PchDMOS transistor." Accordingly, the claim language is appropriate as it stands, and Applicants request withdrawal of this objection.

Claims 1 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,386,135 to Nakazato et al. ("Nakazato"). The rejection is traversed, and reconsideration is requested.

The present invention relates to a semiconductor device including both DMOS and CMOS transistors on a single substrate. Claims 1 and 8 each require a DMOS transistor and a CMOS transistor disposed on one substrate.

Nakazato provides no teaching or suggestion of the claimed "DMOS transistor" as recited by claims 1 and 8. The Office Action relies on the pMOS transistor "pMOS3" in

Nakazato's FIG. 33 as teaching the DMOS transistor, but this is inaccurate. pMOS3 is the p-channel transistor complement to nMOS3, to form a CMOS structure. pMOS3 does not relate to a DMOS transistor, and in fact, Nakazato provides no teaching whatsoever with respect to DMOS transistors.

For at least these reasons, Nakazato does not anticipate the claimed invention, as embodied by claims 1 and 8. Withdrawal of the rejection is requested.

Caim 15 stands rejected under 35 U.S.C. § 103(a) as being obvious over Nakazato. The rejection is traversed and reconsideration is requested.

In order to present a prima facie case of obviousness, the cited reference (or references if combined) must teach every element recited by the claim. Similar to claims 1 and 8 discussed above, claim 15 recites "a p-channel DMOS transistor. . . disposed on the P-type semiconductor substrate. . .[and] a CMOS transistor disposed on the P-type semiconductor substrate." Nakazato provides no teaching or suggestion of a DMOS transistor on a substrate with a CMOS transistor. For at least this reason, Nakazato does not render obvious the claimed invention as embodied by claim 15.

Based on the foregoing, applicants believe the application, including at least claims 1-21 and 23, is in condition for immediate allowance.

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Respectfully submitted,

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